RECEIVED
CENTRAL FAX CENTER
AUG 16 2007

In the Claims:

Please amend claims 1-2 and 4-11, cancel claim 3, and add new claims 12-14 as indicated below. This listing of claims replaces all prior versions.

1. (Currently amended) An electronic circuit comprising:

a plurality of storage elements ~~(101-105)~~ arranged for storing ~~of~~ data elements,

a plurality of processing elements arranged for processing the data elements stored in the plurality of storage elements; and

a timing circuit arranged to determine a first set of points in time, in a first operating mode, at which respective ~~, wherein~~ storage elements of the plurality of storage elements ~~are further arranged to~~ load their data elements, the ~~at respective~~ points in time of [[a]] the first set of points in time~~, and wherein the points in time are~~ being mutually different in order to meet a maximum allowable value of ~~the~~ power consumption peaks, the timing circuit further arranged to determine a second set of points in time, in a second operating mode, at which respective storage elements of the plurality of storage elements load their data elements, the points in time of the second set of points in time being essentially identical, and wherein the timing circuit selects one of the first and second operating modes in response to a control signal.

2. (Currently amended) An electronic circuit according to claim 1, ~~wherein~~ the electronic circuit further comprising[[es]]:

a clock generator arranged to generate a periodic clock signals ~~(111)~~,

delay elements ~~(107, 109)~~ arranged to generate [[a]] points in time of the first set of points in time for [[a]] respective ones of the storage elements to load their data elements by adding respective delays to ~~a source~~ the periodic clock signal, wherein the respective delays are mutually different, and ~~wherein~~ the frequency of the clock generator is low enough in order to ensure data integrity during processing of the data elements.

3. (Canceled) An electronic circuit according to claim 1, further comprising a timing circuit arranged to determine the first set of points in time in a first operating mode, wherein the timing circuit is further arranged to determine a second set of points in time,

in a second operating mode, at which respective storage elements of the plurality of storage elements load their data elements, wherein the respective points in time of the second set of points in time are essentially identical, and wherein the timing circuit is further arranged to select an operating mode depending on a control signal (CS).

4. (Currently amended) An electronic circuit according to claim 1 [[3]], wherein the timing circuit ~~comprises~~ includes

a first clock generator arranged to generate a first periodic clock signals ~~(219), each~~ that is used to determine ~~the respective points in time of~~ the first set of points in time, and ~~wherein the timing circuit further comprises~~

a second clock generator arranged to generate a second periodic clock signals ~~(217), each~~ that is used to determine ~~the respective points in time of~~ the second set of points in time.

5. (Currently amended) An electronic circuit according to claim 4, further comprising:

delay elements ~~(207, 209)~~ arranged to generate [[a]] points in time of the first set of points in time for [[a]] respective ones of the storage elements to load their data elements by adding respective delays to ~~a source~~ the first periodic clock signal ~~(219)~~, wherein the respective delays are mutually different.

6. (Currently amended) An electronic circuit according to claim 1 [[3]], wherein the timing circuit ~~comprises~~ includes a clock generator arranged to generate a periodic clock signals ~~(325), each~~ that is used to determine ~~the respective points in time of~~ either the first set of points in time or the second set of points in time, depending on the control signal ~~(CS)~~.

7. (Currently amended) An electronic circuit according to claim 1, wherein the electronic circuit is a self-timed circuit, further comprising:

a handshake channel ~~(507)~~ arranged for communication between storage elements of the plurality of storage elements and processing elements of the plurality of processing elements, and

delay elements ~~(107, 109)~~ arranged to generate ||a|| points in time of the first set of points in time for [[a]] respective ones of the storage elements by adding respective delays to a request signal for loading of the data elements, wherein the respective delays are mutually different.

8. (Currently amended) An electronic circuit according to claim 1, wherein the electronic circuit is a self-timed circuit, further comprising:

handshake channels ~~(607-613)~~ arranged for communication between storage elements ~~(601-605)~~ of the plurality of storage elements and processing elements of the plurality of processing elements,

a first handshake component ~~(SEQ)~~ arranged to receive a request signal, in [[a]] the first operating mode, for loading of data elements and in response thereto to generate [[a]] request signals for ||a|| respective ones of the storage elements of the plurality of storage elements for loading of data elements at respective points in time of the first set of points in time.

9. (Currently amended) An electronic circuit according to claim 8, further comprising:

a second handshake component ~~(PAR)~~ arranged to receive a request signal, in [[a]] the second operating mode, for loading of data elements and in response thereto to generate [[a]] request signals for [[a]] respective ones of the storage elements ~~(701-705)~~ of the plurality of storage elements for loading of data elements, wherein the request signals in the second mode of operation are generated at essentially identical points in time~~, and wherein the electronic circuit is further arranged to select an operating mode depending on a control signal (CS)~~.

10. (Currently amended) A method of processing data elements, the method comprising:

determining a first set of points in time, in a first operating mode, ~~for storing data elements in~~ at which respective storage elements ~~(101-105)~~ of a plurality of storage elements load their data elements, the points in time of the first set of points in time being mutually different in order to meet a maximum allowable value of power consumption peaks;

determining a second set of points in time, in a second operating mode, at which respective storage elements of the plurality of storage elements load their data elements, the points in time of the second set of points in time being essentially identical;

selecting one of the first and second operating modes in response to a control signal; and

generating output data elements each by performing respective logic operation on ~~respective~~ data elements loaded from the respective storage elements. ~~, wherein the points in time of the first set of points in time at which respective storage elements load their data elements are mutually different in order to meet a maximum allowable value of the power consumption peaks.~~

11. (Currently amended) A method of processing data elements according to claim 10, further comprising:

generating a first periodic clock signal that is used to determine the first set of points in time, and

generating a second periodic clock signal that is used to determine the second set of points in time. ~~determining a second set of points in time, in a second operating mode, for storing data elements in respective storage elements of the plurality of storage elements, wherein the points in time of the second set of points in time at which respective storage elements load their data elements are essentially identical, selecting an operating mode, depending on a control signal.~~

12. (New) A method of processing data elements according to claim 10, further comprising:

generating a periodic clock signal that is used to determine one of the first set of points in time and the second set of points in time in response to the control signal.

13. (New) An electronic circuit comprising:

a plurality of storage elements arranged for storing data elements,

a plurality of processing elements arranged for processing the data elements stored in the plurality of storage elements;

a timing circuit arranged to determine a first set of points in time, in a first operating mode, at which respective storage elements of the plurality of storage elements load their data elements, the points in time of the first set of points in time being mutually different in order to meet a maximum allowable value of power consumption peaks, the timing circuit further arranged to determine a second set of points in time, in a second operating mode, at which respective storage elements of the plurality of storage elements load their data elements, the points in time of the second set of points in time being essentially identical;

a first clock generator arranged to generate a first periodic clock signal that is used to determine the first set of points in time; and

a second clock generator arranged to generate a second periodic clock signal that is used to determine the second set of points in time, and

wherein the timing circuit selects one of the first and second operating modes in response to a control signal.

14. (New) An electronic circuit according to claim 13, further comprising:

delay elements arranged to generate points in time of the first set of points in time for respective ones of the storage elements to load their data elements by adding respective delays to the first periodic clock signal, wherein the respective delays are mutually different.